Overview of Circello

Figure 1 of Circello shows a data processing system 5 that includes a processing core 9 and a debug module 10. As shown in Figure 1, several signals are transmitted from the processing core 9 to the debug module 10. A Bus Grant signal may be transmitted from processing core 9 to debug module 10 which is used by CPU 2 of processing core 9 to indicate to debug module 10 that it has been granted use of K-Bus 25 (Col. 29, lines 41-55). Further, a CPU Processor Status (CPST) signal may be transmitted from processing core 9 to debug module 10 that indicates the type of operation currently being executed by data processor 3 (Col. 18, lines 47-53). For example, the CPST signal may indicate when execution of an instruction begins, when execution of an instruction should continue, when data processor 3 enters into a selected mode of operation, when a preselected branch instruction is executed, and when operation of data processor 3 is halted (Col. 18, lines 53-60).

Additionally, several signals may be transmitted from processing core 9 to debug module 10 over K-Bus 25 (Col. 4, lines 62-63). The signals transmitted over K-Bus 25 are KADDR, KDATA, and KCONTROL (Col. 4, lines 63-65). The KADDR signal is used to send instruction addresses accessed during normal operation of data processor 3 to debug module 10 and the KDATA signal is used to send operand values to debug module 10 (col. 18, lines 25-31). Circello does not explicitly disclose how the KCONTROL signal is used.

In summary, in the system of Circello there are five signals transmitted from processing core 9 to debug module 10 (Bus Grant, CPST, KADDR, KDATA, and KCONTROL). Circello discloses that these signals are used to transmit information such as CPU status, instruction addresses, and operand values. **Nowhere does Circello disclose or suggest that operand addresses are sent to debug module 10 via these signals.**

Response to Examiner's Arguments

In Applicants' previous response, Applicants pointed out that Circello does not disclose or suggest, "a communication link coupling the processor and debug circuit, wherein the processor is configured to transmit to the debug circuit through the communication link a plurality of bit values each representing a state of an operation in the processor including at least

an operand address." Applicants noted that although Circello discloses providing an operand value from core 9 to debug circuit 10, Circello does not disclose or suggest providing an operand address.

On page 3, the Office Action states, "It should be noted that, the term 'operand address' is not defined clearly. With the interpretation in light of the specification, 'operand address' is interpreted as instruction address or program counter value because only the instruction address or the program counter does the indication of memory location."

First, Applicants respectfully disagree that term 'operand address' is not clearly defined. The meaning of the term 'operand address' is well-known and clear to those of skill in the art. As explained in Applicants' previous response, an operand address is simply the memory address at which an operand value is stored. Applicants believe that the meaning of the term 'operand address' is clear. If the Examiner maintains that the meaning of this term is not clear, the Examiner is respectfully requested to identify specifically what he believes to be unclear about the term.

Second, Applicants disagree with the statement in the Office Action that the term "operand address" can be interpreted as an instruction address. During the telephone interview of March 21, 2005, the Examiner explained that because an instruction address specifies the memory location of an instruction and because certain instructions include operand addresses, he believed that an operand address is the same as an instruction address.

Applicants respectfully disagree that an operand address can be interpreted as an instruction address. During the telephone interview, Applicants pointed out that although Circello may disclose sending instruction addresses from the core 9 to the debug circuit 10 (e.g., via the KADDR signal), an instruction address is very different from an operand address. An instruction address specifies the memory location of an instruction, while an operand address specifies the memory location of an operand on which the instruction operates. These two addresses are **different** memory locations. The operand value is stored at a **different** memory location from the instruction. Thus, the operand address is different from the instruction address.

Applicants do not deny that Circello discloses sending **instruction addresses** from the processing core 9 to the debug circuit 10 (i.e., using the KADDR signal over K-Bus 25).

However, these instructions addresses do not include operand addresses, but rather indicate the memory location at which instructions stored. The instruction addresses do not indicate the memory location at which the operands are stored and the operand addresses are not transferred from processing core 9 to debug circuit 10.

The Office Action further asserts that the DDATA signal provided from debug module 10 to external development system 7 discloses providing an operand address from the processor to the debug circuit (*see* Office Action, page 3, *citing* Circello, Col. 15, lines 12-18). Applicants respectfully disagree. First, the DDATA signal is sent from the debug module to an external development system, not from the processor to the debug module. Thus, the DDATA signal is irrelevant to Applicants' claims, which are directed to providing information to the debug circuit from the processor. Second, the DDATA signal provides captured instruction address information. As should be clear from the discussion above, an instruction address is very different from an operand address and does not include an operand address. Thus, while the DDATA signal may provide instruction address, it **does not provide operand addresses**.

Claim 1

Claim 1 is directed to a microcomputer comprising at least one processor, a debug circuit, and a system bus coupling the processor and debug circuit. The microcomputer further comprises a communication link coupling the processor and debug circuit, wherein the processor is configured to transmit to the debug circuit through the communication link a plurality of bit values each representing a state of an operation in the processor including at least an operand address.

As should be clear from the discussion above, Circello does not disclose or suggest, "a communication link coupling the processor and debug circuit, wherein the processor is configured to transmit to the debug circuit through the communication link a plurality of bit values each representing a state of an operation in the processor including at least an operand address." As discussed above, none of the five signals provided from the core 9 to the debug module 10 in Circello (i.e., Bus Grant, CPST, KADDR, KDATA, and KCONTROL) send operand address information to debug module 10.

There is no teaching of the claimed operand address in this portion of Circello. Thus, claim 1 patentably distinguishes over Circello. Accordingly, Applicants respectfully request that the rejection of claim 1 under 35 U.S.C. §102(b) be withdrawn.

Claims 2-20 and claim 61 depend from claim 1, and are allowable for at least the same reasons.

Claim 21

Claim 21 is directed to a microcomputer implemented on a single integrated circuit. The microcomputer comprises, *inter alia*, at least one processor, a debug circuit, a system bus coupling the processor and debug circuit, and a communication link coupling the processor and debug circuit, wherein the processor is configured to transmit to the debug circuit through the communication link a plurality of bit values each representing a state of an operation in the processor including at least one of an operand address and an operand value.

As should be clear from the discussion above, Circello does not teach a processor configured to transmit to the debug circuit through the communication link a plurality of bit values each representing a state of an operation in the processor including at least one of an operand address and an operand value. Accordingly, Applicants respectfully request that the rejection of claim 21 under 35 U.S.C. §102(b) be withdrawn.

Claim 62 depends from claim 21 and is allowable for at least the same reasons.

Claim 22

Claim 22 is directed to a microcomputer comprising, at least one processor, a debug circuit, and a system bus coupling the processor and debug circuit. The microcomputer further comprises means for transmitting to the debug circuit a plurality of bit values each representing a state of an operation in the processor including at least an operand address.

As should be clear from the discussion above, Circello fails to teach means for transmitting to the debug circuit a plurality of bit values **including at least an operand address**. Thus, Applicants respectfully request that the rejection of claim 22 under 35 U.S.C. §102(b) be withdrawn.

Claims 23-41 and claim 63 depend from claim 22 and are allowable for at least the same reasons.

Claim 42

Claim 42 is directed to a method for transferring information between a processor and a debug circuit over a communication link. The method comprises transmitting to the debug circuit a plurality of bit values each representing a state of an operation in the processor including at least an operand address. The method further comprises transmitting a program counter value indicating the program counter of the processor.

As should be clear from the discussion above, Circello does not teach transmitting to the debug circuit a plurality of bit values each representing a state of an operation in the processor **including at least an operand address** . Accordingly, Applicants respectfully request that the rejection of claim 42 under 35 U.S.C. §102(b) be withdrawn.

Claims 43-60 and claim 64 depend from claim 42 and are allowable for at least the same reasons.

CONCLUSION

In view of the foregoing amendments and remarks, this application should now be in condition for allowance. A notice to this effect is respectfully requested. If the Examiner believes, after this amendment, that the application is not in condition for allowance, the Examiner is requested to call the Applicant's attorney at the telephone number listed below.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,

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